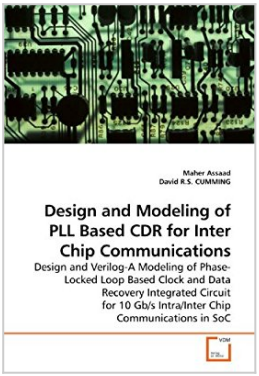

Design and Modeling of PLL Based CDR for Inter Chip Communications: Design and Verilog-A Modeling of Phase-Locked Loop Based Clock and Data Recovery ... Gb/s Intra/Inter Chip Communications in SoC

By Maher Assaad

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This work describes the design and implementation of a fully monolithic 10 Gb/s phase and frequency-locked loop based clock and data recovery (PFLL-CDR) integrated circuit, as well as the Verilog-A modeling of an asynchronous serial link based chip to chip communication system incorporating the proposed concept. The frequency-locked loop (FLL) operates independently from the phase-locked loop (PLL), and has a highly-desired feature that once the proper frequency has been acquired, the FLL is automatically disabled and the PLL will take over to adjust the clock edges approximately in the middle of the incoming data bits for proper sampling. Another important feature of the proposed quarter-rate concept is the inherent 1-to-4 demultiplexing of the input serial data stream. In order to verify the accuracy of the proposed quarter-rate concept, a clockless asynchronous serial link incorporating the proposed concept and communicating two chips at 10 Gb/s has been modeled at gate level using the Verilog-A language and time-domain simulated.

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Editorial Review

About the Author
I was born in Syria, completed my B.Sc. in Mathematics and Physics at Tishreen University in Syria, my M.Eng. in Electrical Engineering at the University of Montreal in Canada, and my Ph.D. in Electrical Engineering at the University of Glasgow in the U.K.

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